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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/562,887	12/29/2005	Sergei Sawitzki	NL 030780	6932

65913 7590 10/23/2009

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EXAMINER	
ELMORE, REBA I	

ART UNIT	PAPER NUMBER
2189	

NOTIFICATION DATE	DELIVERY MODE
10/23/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/562,887	SAWITZKI ET AL.	
	Examiner	Art Unit	
	Reba I. Elmore	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 August 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6,8-16 and 21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *16 and 21* is/are allowed.

6)☒ Claim(s) *1,2,4-6,8 and 10* is/are rejected.

7)☒ Claim(s) *3,9 and 11-15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-6, 8-16 and 21 have been presented for examination. Claims 7 and 17-20 were canceled.

2. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

SPECIFICATION

3. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

35 USC 102

4. The rejection of claims 1-2, 4-6, 8 and 10 is ***maintained*** and repeated below.

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1-2, 4-6, 8 and 10 are rejected under 35 U.S.C. 102(e) as being anticipated by Sevalia et al. (P.N 6,526,495).

7. Sevalia teaches the present invention (claim 1) as claimed including a memory device comprising:

a. a memory having at least two predetermined register memory sections addressable by respective address ranges (e.g. see the abstract and col. 1, lines 25-36);

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b. at least one access port for providing access to the memory as the memory device being a multiport FIFO (e.g. see Figure 1 and col. 1, lines 25-36);

c. access control means for addressing the memory (e.g. see Figure 1, element 107 so as to operate the register memory sections as shift registers and to map shift register accesses of at least one access port to predetermined addresses in a global address space of the memory, the control means being external to the memory and being configured to generate memory addresses for writing to and reading from the memory as the FIFOs being equivalent to shift registers (e.g. see Figure 1); and,

d. a buffer memory connectable to at least one access port and to the memory, wherein a line width of the buffer memory and the memory is selected to be greater or equal the data width of at least one access port multiplied by the sum of read accesses and write accesses per cycle as using several FIFOs which are implemented with different data widths and/or depths (e.g. see col. 2, lines 18-38).

As to claim 2, Sevalia teaches the present invention wherein the access control means comprises at least one address counter as the input to the circuit (e.g. see Figure 8 with support at col. 4, line 60 to col. 5, line 8).

As to claim 4, Sevalia teaches the present invention wherein at least one access port provides access to a plurality of data sources for writing data to respective register memory sections, and to a plurality of data processing devices for reading data from the register memory sections as multiplexers which direct reading or writing data to a particular buffer memory (e.g. see Figure 8).

As to claim 5, Sevalia teaches the present invention wherein the access control means is arranged to provide alternate access for the data sources and the data processing devices as a

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control means which access a given buffer as a data source (e.g. see Figure 1).

As to claim 6, Sevalia teaches the present invention wherein data sources accesses are controlled to cycle through the global address space and processing device accesses are controlled to cycle through the address range of a respective register memory section (e.g. see Figure 8 with support at col. 4, line 60 to col. 5, line 8).

As to claim 8, Sevalia teaches the present invention wherein the memory is a single-port memory as shown in Figure 8 with 1A being an input port.

As to claim 10, Sevalia teaches the present invention wherein the buffer memory is arranged to buffer read and write accesses of at least one access port (e.g. see col. 2, line 61 to col. 3, line 9).

ALLOWABLE SUBJECT MATTER

8. Claims 3, 9 and 11-15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

9. Claims 16 and 21 read over the art of record.

RESPONSE TO APPLICANT'S REMARKS

10. Applicant's arguments filed August 18, 2009 have been fully considered but they are not persuasive.

11. As to the Sevalia reference not teaching "memory having at least two predetermined register memory sections addressable by respective address ranges', the cite given for the address ranges discusses the data input to the storage queues is a data stream which is equivalent to an address range. It is inherent that the address ranges are addressable or accessible to the active

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elements of the system.

12. As to the reference not teaching the buffer memory coupled to the memory because the FIFOs queues are included in the memory, the Leong reference which was incorporated by reference in col. 2, lines 39-60 and therefore within the four corners of the Sevalia references shows both buffers and system memory as being different but connected entities. This element is taught to the extent claimed by the actual claim language.

13. As to the data width not be taught by the Sevalia reference, the reference teaches the data widths and depths are flexible elements of the FIFO structure of the invention as taught. This element is taught to the extent claimed by the actual claim language.

CONCLUSION

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Reba I. Elmore, whose telephone number is (571) 272-4192. The examiner can normally be reached on Monday and Thursday from 7:30am to 6:00pm, EST.

If attempts to reach the examiner by telephone are unsuccessful, the art unit supervisor for AU 2189, Reginald G. Bragdon, can be reached for general questions concerning this application at (571) 272-4204. Additionally, the official fax phone number for the art unit is (571) 273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Tech Center central telephone number is (571) 272-2100.

/Reba I. Elmore/
Primary Patent Examiner
Art Unit 2189

Tuesday, October 20, 2009

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